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FERNANDO GONZALEZ

DAVID CHAPEK

and

RANDHIR P. S. THAKUR

for

METHOD FOR FORMING A SELF-ALIGNED ISOLATION TRENCH

WORKMAN, NYDEGGER & SEELEY
A PROFESSIONAL CORPORATION
ATTORNEYS AT LAW
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UTAH 84111

1 This is a continuation of U.S. Patent Application Serial No. 08/985,588, filed on
2 December 5, 1997, which is a divisional patent application of U.S. Patent Application Serial
3 Number 08/823,609, filed on March 25, 1997, both of which are incorporated herein by
4 reference.

5

6 **BACKGROUND OF THE INVENTION**

7 1. **The Field of the Invention**

8 The present invention relates to forming an isolation trench in a semiconductor
9 device. In particular, the present invention relates to a method of forming an isolation trench
10 in an etching process for a semiconductor device that combines a spacer etch with a trench
11 etch.

12

13 2. **The Relevant Technology**

14 An isolation trench is used in an active area associated with a microelectronic device
15 on a semiconductor substrate or on a substrate assembly. Isolation trenches allow
16 microelectronics devices to be placed increasingly closer to each other without causing
17 detrimental electronic interaction such as unwanted capacitance build-up and cross-talk. In
18 the context of this document, the term semiconductive substrate is defined to mean any
19 construction comprising semiconductive material, including but not limited to bulk
20 semiconductive material such as a semiconductive wafer, either alone or in assemblies
21 comprising other materials thereon, and semiconductive material layers, either alone or in
22 assemblies comprising other materials. The term substrate refers to any supporting structure
23 including but not limited to the semiconductive substrates described above. The term
24 substrate assembly is intended herein to mean a substrate having one or more layers or
25 structures formed thereon. As such, the substrate assembly may be, by way of example and

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1 not by way of limitation, a doped silicon semiconductor substrate typical of a semiconductor
2 wafer.

3 The ever-present pressure upon the microelectronics industry to shrink electronic
4 devices and to crowd a higher number of electronic devices onto a single die, called
5 miniaturization, has required the use of such structures as isolation trenches.

6 In the prior state of the art, an etching process of fill material within an isolation
7 trench has been problematic. As seen in Figure 1, a semiconductor substrate 12 has an
8 isolation trench substantially filled up with an isolation material 48. A pad oxide 14 is
9 situated on the active area of semiconductor substrate 12. Isolation material 48 exhibits a
10 non-planarity at the top surface thereof between corners 62, particularly as is seen at
11 reference numeral 46 in Figure 1. The non-planarity of the top surface of isolation
12 material 48 is due to dissimilarity of etch rates between isolation material 48 and pad
13 oxide 14, particularly at corners 62 of the active area of semiconductor substrate 12.

14 An active area may be formed within semiconductor substrate 12 immediately
15 beneath pad 14, and adjacent isolation material 48. A problem that is inherent in such non-
16 planarity of fill material within an isolation trench is that corners 62 may leave the active area
17 of semiconductor substrate 12 exposed. As such, isolation material 48 will not prevent layers
18 formed thereon from contacting the active area of semiconductor substrate 12 at corners 62.
19 Contact of this sort is detrimental in that it causes charge and current leakage. Isolation
20 material 48 is also unable to prevent unwanted thermal oxide encroachment through corners
21 62 into the active area of semiconductor substrate 12.

22 What is needed is a method of forming an isolation trench, where subsequent etching
23 of fill material within the isolation trench of such method prevents overlying layers from
24 having contact with an adjacent active area, and prevents unwanted thermal oxide
25 encroachment into the active area. What is also needed is a method of forming an isolation
26 trench wherein etching or planarizing such as by chemical mechanical planarization (CMP)

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SALT LAKE CITY, UTAH 84111

1 of isolation trench materials is accomplished without forming a recess at the intersection of
2 the fill material in the isolation trench and the material of the active area within the
3 semiconductor substrate.

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SUMMARY OF THE INVENTION

2 The present invention relates to a method for forming an isolation trench structure
3 on a semiconductor substrate. The inventive method forms and fills the isolation trench
4 without causing deleterious topographical depressions in the upper surface of the fill material
5 in the isolation trench, while substantially preventing contact between layers overlying the
6 fill material of the isolation trench and the active area of the semiconductor substrate. By
7 avoiding such deleterious topographical depressions and the exposure of the active area,
8 detrimental charge and current leakage is minimized.

9 The inventive method of forming an isolation trench comprises forming a pad oxide
10 upon a semiconductor substrate and depositing a first dielectric layer thereupon. By way of
11 non-limiting example, the first dielectric layer is a nitride layer. The first dielectric layer is
12 patterned and etched with a mask to expose a portion of the pad oxide layer and to protect
13 an active area in the semiconductor substrate that remains covered with the first dielectric
14 layer. A second dielectric layer is formed substantially conformably over the pad oxide layer
15 and the remaining portions of the first dielectric layer.

16 A spacer etch is used to form a spacer from the second dielectric layer. The spacer
17 electrically insulates the first dielectric layer. An isolation trench etch follows the spacer etch
18 and creates within the semiconductor substrate an isolation trench that is defined by surfaces
19 in the semiconductor substrate. The spacer formed by the spacer etch facilitates self-
20 alignment of the isolation trench formed by the isolation trench etch. The isolation trench
21 etch can be carried out with the same etch recipe as the spacer etch, or it can be carried out
22 with an etch recipe that is selective to the spacer. Once the isolation trench is formed, an
23 insulation liner on the inside surface of the isolation trench can be optionally formed, either
24 by deposition or by thermal oxidation.

25 A third dielectric layer is formed substantially conformably over the spacer and the
26 first dielectric layer so as to substantially fill the isolation trench. Topographical reduction

1 of the third dielectric layer follows, preferably so as to planarize the third dielectric layer for
2 example by chemical mechanical planarizing (CMP), by dry etchback, or by a combination
3 thereof.

4 The topographical reduction of the third dielectric layer may also be carried out as
5 a single etchback step that sequentially removes superficial portions of the third dielectric
6 layer that extend out of the isolation trench. The single etchback also removes portions of
7 the remaining spacer, and removes substantially all of the remaining portions of the first
8 dielectric layer. Preferably, the single etchback will use an etch recipe that is more selective
9 to the third dielectric layer and the spacer than to the remaining portions of the first dielectric
10 layer. The single etchback uses an etch recipe having a selectivity that will preferably leave
11 a raised portion of the third dielectric layer extending above the isolation trench while
12 removing substantially all remaining portions of the first dielectric layer. The resulting
13 structure can be described as having the shape of a nail as viewed in a direction that is
14 substantially orthogonal to the cross section of a word line in association therewith.

15 Several other processing steps are optional in the inventive method. One such
16 optional processing step is the deposition of a polysilicon layer upon the pad oxide layer to
17 act as an etch stop or planarization marker. Another optional processing step includes
18 clearing the spacer following the isolation trench etch. An additional optional processing
19 step includes implanting doping ions at the bottom of the isolation trench to form a doped
20 trench bottom. When a CMOS device is being fabricated, the ion implantation process may
21 require a partial masking of the semiconductor substrate so as to properly dope selected
22 portions of the semiconductor substrate.

23 These and other features of the present invention will become more fully apparent
24 from the following description and appended claims, or may be learned by the practice of the
25 invention as set forth hereinafter.
26

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages of the invention are obtained, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Figure 1 illustrates the prior art problem of an uneven etch of an isolation trench that results in exposing portions of an active area and unwanted thermal oxide encroachment into the active area.

Figure 2A is an elevational cross-section view of a semiconductor substrate, wherein a pad oxide and a nitride layer have been deposited upon the semiconductor substrate.

Figure 2B is an elevational cross-section view of a semiconductor substrate having thereon a polysilicon layer that has been deposited upon a pad oxide, and a nitride layer that has been deposited upon the polysilicon layer.

Figure 3A illustrates further processing of the structure depicted in Figure 2A, wherein a mask has been patterned and the nitride layer has been etched down to the pad oxide layer to form a nitride island over future or current active areas in the substrate that are to be protected.

Figure 3B illustrates further processing of the structure depicted in Figure 2B, wherein a mask has been patterned and the nitride layer has been etched down through the nitride layer and the polysilicon layer to stop on the pad oxide layer, thereby forming a nitride island and a polysilicon island over future or current active areas in the substrate that are to be protected.

1 Figure 4A is a view of further processing of Figure 3A, wherein the mask has been
2 removed and an insulation film has been deposited over the nitride island.

3 Figure 4B illustrates further processing of the structure in Figure 3B, wherein the
4 mask has been removed and an insulation film has been deposited over the nitride island and
5 the polysilicon island.

6 Figures 5A and 5B illustrate further processing of the structure depicted, respectively,
7 in Figures 4A and 4B, in which the insulation film has been etched to form a spacer, a
8 simultaneous or serial etch has formed an isolation trench, thermal oxidation or deposition
9 within the isolation trench has formed an insulation liner therein, and wherein an optional
10 ion implantation has formed a doped region at the bottom of the isolation trench.

11 Figures 6A and 6B illustrate further processing of the structure depicted, respectively,
12 in Figures 5A and 5B, in which an isolation film has been deposited over the spacer, the
13 isolation trench within the isolation trench liner, and the nitride island.

14 Figures 7A and 7B illustrate further processing of the structure depicted, respectively,
15 in Figures 6A and 6B, wherein a planarization process has formed a first upper surface made
16 up of the nitride island, the spacer, and the isolation film, all being substantially co-planar
17 on the first upper surface.

18 Figure 8A illustrates further processing of the structure depicted in Figures 7A or 9A,
19 wherein the semiconductor substrate has been implanted with ions, and wherein the isolation
20 film, optionally the pad oxide layer, the insulation liner, and the spacer have fused to form
21 a unitary isolation structure.

22 Figure 8B illustrates optional further processing of the structure depicted in
23 Figure 6B, wherein an etching process using an etch recipe that is slightly selective to oxide
24 over nitride, has etched back the isolation film, the nitride island, and the spacer to expose
25 the polysilicon island, and has formed a filled isolation trench which, when viewed in a

1 direction that is substantially orthogonal to the cross section of the depicted word line, has
2 the shape of a nail.

3 Figure 9A illustrates optional further processing of the structure depicted in
4 Figure 6A or in Figure 7A, wherein an etch-selective recipe that is slightly selective to oxide
5 over nitride has formed a filled isolation trench which, when viewed in cross section, has the
6 shape of a nail.

7 Figure 9B illustrates further processing of the structure depicted in either Figures 7B
8 or 8B wherein the semiconductor substrate has been implanted with ions, and wherein the
9 isolation film, optionally the pad oxide layer, the insulation liner, and the spacer have been
10 fused to form a filled isolation trench.

1 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

2 The present invention relates to a method for forming a self-aligned isolation trench.
3 The isolation trench is preferably a shallow trench isolation region that is self-aligned to an
4 underlying active area. Stated otherwise, the inventive method forms a Narrow self-aligned
5 Active area Isolation region that is inherently Level (NAIL). In the method of the present
6 invention, a spacer etch and an isolation trench etch can be accomplished essentially within
7 the same processing step.

8 Another aspect of the present invention relates to a combined nitride and oxide etch
9 that is selective to polysilicon, and in which selectivity of the etch between nitride and oxide
10 materials favors one or the other by a factor of about one half. A still further aspect of the
11 present invention relates to the use of a polysilicon film as an etch stop or planarization
12 marker film. The structure achieved by the method of the present invention achieves
13 particular advantages that overcome problems of the prior art.

14 A starting structure for an example of a first embodiment of the present invention is
15 illustrated in Figure 2A. In Figure 2A, a pad oxide 14 is grown upon a semiconductor
16 substrate 12 on a semiconductor structure 10. Semiconductor substrate 12 can be
17 substantially composed of silicon. Following growth of pad oxide 14, a nitride layer 16 is
18 deposited over semiconductor substrate 12. Figure 2A illustrates deposition of nitride
19 layer 16 upon pad oxide 14.

20 Figure 3A illustrates a step in the formation of an isolation trench by the method of
21 the present invention. Nitride layer 16 is patterned with a mask 20. An anisotropic etch
22 selectively removes portions of nitride layer 16. Figure 3A illustrates the result of etching
23 with the use of mask 20, wherein nitride layer 16 has formed an insulator island 22, as seen
24 in Figure 4A. Insulator island 22 is patterned over and protects future or current active areas
25 (not pictured) in semiconductor substrate 12 during isolation trench processing. Following
26 etch of nitride layer 16, mask 20 is removed.

1 Figure 4A illustrates further processing of the structure depicted in Figure 3A,
2 wherein an insulation film 26 has been deposited upon insulator island 22 and exposed
3 portions of pad oxide 14. Insulation film 26 can be an oxide such as silicon dioxide, and can
4 be formed for example by decomposition of tetraethyl ortho silicate (TEOS). Insulation
5 film 26 may also be formed by a plasma enhanced chemical vapor deposition (PECVD)
6 process so as to deposit a nitride layer such as Si₃N₄ or equivalent. When insulation film 26
7 is a nitride layer, insulator island 22 would be selected to be composed of a substantially
8 different material, such as an oxide. Formation of substantially different materials between
9 insulator island 22 and insulation film 26 facilitate selective etchback or selective mechanical
10 planarization such as chemical-mechanical polishing (CMP) in the inventive method of
11 forming an isolation trench.

12 Following deposition of insulation film 26, a spacer etch and an isolation trench etch
13 are carried out. The spacer etch and the isolation trench etch can be carried out with a single
14 etch recipe that is selective to insulation film 26. Alternatively, the spacer etch and the
15 isolation trench etch can be carried out with two etch recipes. As such, the first etch etches
16 insulation film 26 in a spacer etch that forms a spacer 28 seen in Figure 5A. The second
17 etch, or isolation trench etch, has an etch recipe that is selective to spacer 28 and insulator
18 island 22, and anisotropically etches an isolation trench 32 having a side wall 50 in
19 semiconductor substrate 12.

20 Spacer 28 may facet during the spacer etch such that a substantially linear spacer
21 profile is achieved. Spacer 28 adds the advantage to the inventive process of extending the
22 lateral dimension of the active area that is to be formed within semiconductor substrate 12
23 immediately beneath insulator island 22. Because spacer 28 takes up lateral space that would
24 otherwise be available for isolation trench 32, isolation trench 32 is made narrower and the
25 active area that is to be formed within semiconductor substrate 12 is made wider.

26 * see p.15 "selective to"

Following the formation of isolation trench 32, sidewall 50 of isolation trench 32 has optionally formed thereon an insulation liner 30. For example, thermal oxidation of sidewall 50 will form insulation liner 30 within isolation trench 32. Insulation liner 30 will preferably be substantially composed of silicon dioxide. In Figure 5A it can be seen that, following thermal oxidation of sidewall 50 to form insulation liner 30 within isolation trench 32, semiconductor substrate 12 forms a rounded edge at the top of isolation trench 32. Rounding of the top of semiconductor substrate 12 at the corners of isolation trench 32 provides an added advantage of further isolating semiconductor substrate 12 immediately beneath insulator island 22; thereby an active area that will form in semiconductor substrate 12 immediately under insulator island 22 will be further isolated. The feature of rounding of the corners of semiconductor substrate 12 at the tops of isolation trenches 32 as depicted in Figures 5A and 5B is presupposed in all embodiments of the present invention as a preferred alternative.

Another method of forming insulation liner 30 is CVD of a dielectric material, or a dielectric material precursor that deposits preferentially upon sidewall 50 of isolation trench 32. The material of which insulation liner 30 is substantially composed may be particularly resistant to further etching, cleaning, or other processing conditions.

Insulation liner 30 may be substantially composed of a nitride such as Si_3N_4 , or an equivalent, and can be selectively formed upon sidewall 50 of isolation trench 32. When semiconductor substrate 12 immediately adjacent to isolation trench 32 is a doped monocrystalline silicon that forms, for example, an active area for a transistor source/drain region, oxidation is avoided therein by insulation liner 30. Insulation liner is preferably substantially composed of Si_3N_4 or a non-stoichiometric variant which seals sidewall 50 so as to prevent encroachment of oxide into semiconductor substrate 12.

Following formation of insulation liner 30, ion implantation is optionally carried out to form a doped trench bottom 34 at the bottom of isolation trench 32. For example, if

1 semiconductor wafer 10 comprises an N-doped silicon substrate, implantation of P-doping
2 materials at the bottom of isolation trench 32 will form a P-doped trench bottom 34. Ion
3 implantation may be carried out in a field implantation mode. If a complementary metal
4 oxide semiconductor (CMOS) is being fabricated, however, masking of complimentary
5 regions of semiconductor substrate 12 is required in order to achieve the differential doping
6 thereof. For an N-doped silicon substrate, a high breakdown voltage may be achieved by P-
7 doping. A low breakdown voltage may ^{be} achieved by N-doping, and an intermediate
8 breakdown voltage may be achieved by no doping. Because the present invention relates to
9 formation of isolation trenches, P-doping in an N-well region, or N-doping in a P-well region
10 are preferred.

11 Preferably, implantation of P-doping ions is carried out to form doped trench
12 bottom 34 in a direction that is substantially orthogonal to the plane of pad oxide 14.
13 Slightly angled implantation of P-implantation ions may be carried out to enrich or broaden
14 the occurrence of P-doping ions in doped trench bottom 34 at the bottom of isolation
15 trench 32. If P-doping is carried out where semiconductor substrate 12 is N-doped, care must
16 be taken not to dope through insulation liner 30 on sidewall 50 near pad oxide 14, which may
17 cause detrimental deactivation of active areas (not shown) in semiconductor substrate 12.

18 Following optional implantation of doping ions, it may be desirable, depending upon
19 the intended shape and design of the isolation trench, to remove all or a portion of spacer 28.
20 The isolation trench formed by the inventive method, however, will preferably include at
21 least a portion of spacer 28 that extends away from the isolation trench 32.

22 As seen in Figure 6A, isolation trench 32 is filled by an isolation film 36 which also
23 is formed upon insulator island 22. Isolation film 36 can be formed by a deposition process
24 using, for example, TEOS as a precursor.

25 An optional processing step of the inventive method is to fuse together spacer 28, pad
26 oxide 14, and isolation film 36. The processing technique for such fusion is preferably a heat

1 treatment of semiconductor structure 10. If such fusion is contemplated, it is also desirable
2 that spacer 28, pad oxide 14, and isolation film 36 all be composed of substantially the same
3 material, as fusion is best facilitated with common materials.

4 It is preferable, at some point in fabrication of the isolation trench, to densify the fill
5 material of the isolation trench. Densification is desirable because it helps to prevent
6 separation of materials in contact with the fill material. As seen in Figure 6A, densification
7 will prevent isolation film 36 from separating at interfaces with spacer 28, pad oxide
8 layer 14, and insulation liner 30. It is preferable to perform densification of isolation film 36
9 immediately following its deposition. Depending upon the specific application, however,
10 densification may be carried out at other stages of the process. For example, densification
11 of isolation film 36 by rapid thermal processing (RTP) may make either etchback or CMP
12 more difficult. As such, it is preferable to densify later in the fabrication process, such as
13 after planarizing or etchback processing.

14 Figure 7A illustrates a subsequent step of formation of the isolation trench wherein
15 insulator island 22, spacer 28, and isolation film 36 are planarized to a common co-planar
16 first upper surface 38. First upper surface 38 will preferably be formed by a CMP or
17 etchback process. Preferably, planarization will be selective to isolation film 36, and
18 relatively slightly selective to insulator island 22, such as by a factor of about one half.¹⁴ A
19 first preferred selectivity of an etch recipe used in the inventive method is in the range of
20 about 1:1 to about 2:1, selective to isolation film 36 as compared to insulator island 22.¹⁴ A
21 more preferred selectivity is in the range of about 1.3:1 to about 1.7:1. A most preferred
22 selectivity is about 1.5:1. Planarization also requires the etch recipe to be slightly selective
23 to spacer 28 over insulator island 22. Preferably, spacer 28 and isolation film 36 are made
24 from the same material such that the etch will be substantially uniform as to the selectivity
25 thereof with respect to spacer 28 and isolation film 36 over insulator island 22.¹⁴

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1 First upper surface 38 is illustrated as being substantially planar in Figure 7A. It will
2 be appreciated by one of ordinary skill in the art that first upper surface 38 will form a
3 nonplanar profile or topography depending upon the selectivity of the etch recipe or of the
4 chemical used in a planarization technique such as CMP. For example, where reduced island
5 52 is formed from a nitride material and isolation film 36 is formed from an oxide material,
6 first upper surface 38 would undulate as viewed in cross section with more prominent
7 structures being the result of an etch or planarization technique more selective thereto.

8 In Figure 7A, reduced island 52 has been formed from insulator island 22.
9 Additionally, portions of isolation film 36 and spacer 28 remain after planarization. Reduced
10 island 52 preferably acts as a partial etch stop.

11 Figure 8A illustrates the results of removal of reduced island 52. Reduced island 52
12 is preferably removed with an etch that is selective to isolation film 36 and spacer 28, leaving
13 an isolation structure 48 that extends into and above isolation trench 32, forming a nail
14 shaped structure having a head 54 extending above and away from isolation trench 32 upon
15 an oxide layer 44. The future or current active area of semiconductor substrate 12, which
16 may be at least partially covered over by head 54, is substantially prevented from a
17 detrimental charge and current leakage by head 54.

18 Phantom lines 60 in Figure 8A illustrate remnants of pad oxide layer 14, insulation
19 liner 30, and spacer 28 as they are optionally thermally fused with isolation film 36 to form
20 isolation structure 48. Isolation structure 48, illustrated in Figure 8A, comprises a trench
21 portion and a flange portion which together, when viewed in cross section, form the shape
22 of a nail.

23 The trench portion of isolation structure 48 is substantially composed of portions of
24 isolation film 36 and insulation liner 30. The trench portion intersects the flange portion at
25 a second upper surface 40 of semiconductor substrate 12 as seen in Figure 8A. The trench
26 portion also has two sidewalls 50. Figure 8A shows that the trench portion is substantially

1 parallel to a third upper surface 42 and sidewalls 50. The flange portion is integral with the
2 trench portion and is substantially composed of portions of pad oxide layer 14, spacer 28,
3 and isolation film 36. The flange portion has a lowest region at second upper surface 40
4 where the flange portion intersects the trench portion. The flange portion extends above
5 second upper surface 40 to third upper surface 42 seen in Figure 8A. Upper surfaces 40, 42
6 are substantially orthogonal to two flange sidewalls 64 and sidewall 50. The flange portion
7 is substantially orthogonal in orientation to the trench portion. The flange portion may also
8 include a gate oxide layer 44 after gate oxide layer 44 is grown.

9 Following formation of isolation structure 48, it is often useful to remove pad
10 oxide 14, seen in Figure 8A, due to contamination thereof during fabrication of isolation
11 structure 48. Pad oxide 14 can become contaminated when it is used as an etch stop for
12 removal of reduced island 52. For example, pad oxide 14 may be removed by using aqueous
13 HF to expose second upper surface 40. A new oxide layer, gate oxide layer 44, may then
14 be formed on second upper surface 40 having third upper surface 42.

15 Semiconductor structure 10 may be implanted with ions as illustrated by arrows seen
16 in Figure 8A. This implantation, done with N-doping materials in an N-well region, for
17 example, is to enhance the electron conductivity of the active area (not shown) of
18 semiconductor substrate 12. Either preceding or following removal of pad oxide 14 seen in
19 Figure 8A, an enhancement implantation into the active area of semiconductor substrate 12
20 may be carried out, whereby preferred doping ions are implanted on either side of isolation
21 structure 48. ✓

22 Ion implantation into semiconductor substrate 12 to form active areas, when carried
23 out with isolation structure 48 in place, will cause an ion implantation concentration gradient
24 to form in the region of semiconductor substrate 12 proximate to and including second upper
25 surface 40. The gradient will form within semiconductor substrate 12 near second upper
26 surface 40 and immediately beneath the flange sidewalls 64 as the flange portion of isolation

1 structure 48 will partially shield semiconductor substrate 12 immediately therebeneath.
2 Thus, an ion implant gradient will form and can be controlled in part by the portion of
3 semiconductor substrate 12 that is covered by head 54.

4 Gate oxide layer 44 is formed upon second upper surface 40 after pad oxide 14 has
5 been removed to form portions of third upper surface 42. The entirety of third upper
6 surface 42 includes head 54 of isolation structure 48 as it extends above gate oxide layer 44
7 and gate oxide layer 44.

8 In a variation of the first embodiment of the present invention, the structure illustrated
9 in Figure 6A is planarized by use of a single etchback process. The single etchback uses an
10 etch recipe that has a different selectivity for insulator island 22 than for isolation film 36.
11 In this alternative embodiment, spacer 28, dielectric film 36, and pad oxide 14 are composed
12 of substantially the same material. Insulator island 22 has a composition different from that
13 of isolation film 36. For example, isolation film 36 and spacer 28 are composed of SiO₂, and
14 insulator island 22 is composed of silicon nitride.

15 The etch recipe for the single etchback is chosen to be selective to isolation film 36
16 such that, as upper surface 58 of isolation film 36 recedes toward pad oxide 14 and
17 eventually exposes insulator island 22 and spacer 28, insulator island 22 has a greater
18 material removal rate than spacer 28 or isolation film 36. As such, a final isolation
19 structure 48 illustrated in Figure 9A is achieved. Pad oxide 14 acts as an etch stop for this
20 etch recipe. A residual depression of isolation film 36 may appear centered over filled
21 isolation trench 32. A depression would be created, centered above isolation trench 32,
22 during the filling of isolation trench 32 with isolation film 36, as seen in Figure 6A. Where
23 a depression is not detrimental to the final isolation structure 48 as illustrated in Figure 9A,
24 this selective etch recipe alternative may be used.

25 Semiconductor structure 10, as illustrated in Figure 9A, can be seen to have a
26 substantially continuous isolation structure substantially covering semiconductor

1 substrate 12. An upper surface 42a of isolation structure 48 includes the head portion or nail
2 head 54. Semiconductor substrate 12 is covered at an upper surface 42b by either a pad
3 oxide layer or a gate oxide layer. Another upper surface 42c comprises the upper surface of
4 the pad oxide layer or gate oxide layer.

5 A starting structure for an example of a second embodiment of the present invention
6 is illustrated in Figure 2B. In Figure 2B, pad oxide layer 14 is grown upon semiconductor
7 substrate 12 and a polysilicon layer 18 is deposited upon pad oxide layer 14. This
8 embodiment of the present invention parallels the processing steps of the first embodiment
9 with the additional processing that takes into account the use of polysilicon layer 18.

10 Figure 3B illustrates etching through nitride layer 16 and polysilicon layer 18 to stop
11 on pad oxide layer 14. The etch creates both an insulator island 22 and a polysilicon
12 island 24 formed, respectively, from nitride layer 16 and polysilicon layer 18.

13 Figure 4B illustrates further processing of the structure depicted in Figure 3B,
14 wherein insulation film 26 has been deposited upon insulator island 22, laterally exposed
15 portions of polysilicon island 24, and exposed portions of pad oxide layer 14. Following
16 deposition of insulation film 26, a spacer etch and an isolation trench etch are carried out
17 similarly to the spacer etch and isolation trench etch carried out upon semiconductor
18 structure 10 illustrated in Figure 5A.

19 Figure 5B illustrates the results of both the spacer etch and the isolation trench etch
20 and optional implantation of isolation trench 32 to form doped well 34 analogous to doped
21 trench bottom 34 illustrated in Figure 5A. Formation of insulation liner 30 within isolation
22 trench 32 preferentially precedes implantation to form doped trench bottom 34. Following
23 optional implantation of doping ions, full or partial removal of spacer 28 may optionally be
24 performed as set forth above with respect to the first embodiment of the invention.

25 Figure 6B illustrates a subsequent step in fabrication of an isolation trench according
26 to the second embodiment of the inventive method, wherein isolation film 36 is deposited

1 both within isolation trench 32, and over both of insulator island 22 and spacer 28. As set
2 forth above, densification of isolation film 36 is a preferred step to be carried out either at
3 this stage of fabrication or at a subsequent selective stage. Planarization or etchback of
4 isolation film 36 is next carried out as set forth in the first embodiment of the present
5 invention, and as illustrated in Figure 7B.

6 The process of planarization or etchback of isolation film 36 reduces insulator
7 island 22 to form reduced island 52 as illustrated in Figure 7B. Next, additional selective ion
8 implantations can be made through polysilicon island 24 and into the active area of
9 semiconductor substrate 12 that lies beneath polysilicon island 24.

10 In Figure 8B, it can be seen in phantom that spacer 28 has a top surface that is co-
11 planar with third upper surface 42 of isolation structure 48 after planarization. Polysilicon
12 island 24 and spacer 28 are formed as shown in Figure 8B. Removal of spacer 28 from the
13 structures illustrated in Figure 8B can be accomplished by patterning and etching with a
14 mask that covers head 54 that extends above and away from isolation trench 32 seen in
15 Figure 8B. The etching process exposes a surface on semiconductor substrate 12 upon which
16 a gate oxide layer is deposited or grown.

17 To form the structure seen in Figure 9B, semiconductor structures 10 of Figures 7B
18 or 8B are subjected to implantation of semiconductor substrate 12 with ions. Semiconductor
19 structure 10 is then subjected to a heat treatment so as to fuse together isolation film 36,
20 optional pad oxide layer 14, insulation liner 60, and spacer 28 into an integral filled isolation
21 trench.

22 Subsequent to the process illustrated in Figures 6A-8A and 6B-9B a final thermal
23 treatment, or subsequent thermal treatments, can be performed. Heat treatment may cause
24 isolation structure 48 to be wider proximal to upper surface 42 than proximal to doped trench
25 bottom 34. When so shaped, an unoxidized portion of the active area of semiconductor
26 substrate 12 that forms sidewall 50 would have a trapezoidal shape when viewed in cross

1 section, where the widest portion is upper surface 40 and the narrowest portion is at doped
2 trench bottom 34. Where a trapezoidal shape of the trench portion causes unwanted
3 encroachment into the active area of semiconductor substrate 12, the optional formation of
4 insulation liner 30 from a nitride material or equivalent is used to act as an oxidation barrier
5 for sidewall 50. Semiconductor structure 10 is illustrated in Figure 9B as being implanted
6 by doping ions, as depicted with downwardly-directed arrows. Following a preferred
7 implantation, thermal processing may be carried out in order to achieve dopant diffusion near
8 upper surface 42b of implanted ions residing within semiconductor substrate 12. Due to
9 head 54 extending onto semiconductor substrate 12, a doping concentration gradient can be
10 seen between the active area 53a and the active area 53b. The starting and stopping point of
11 the doping concentration gradient in relation to flange sidewalls 64 will depend upon the
12 duration and temperature of a thermal treatment.

13 The present invention may be carried out wherein spacer 28 and isolation film 36 are
14 substantially composed of the same oxide material, and insulator island 22 is substantially
15 composed of a nitride composition. Other compositions may be chosen wherein etch
16 selectivity or CMP selectivity slightly favors insulator island 22 over both spacer 28 and
17 isolation film 36. The specific selection of materials will depend upon the application during
18 fabrication of the desired isolation trench.

19 The present invention may be embodied in other specific forms without departing
20 from its spirit or essential characteristics. The described embodiments are to be considered
21 in all respects only as illustrated and not restrictive. The scope of the invention is, therefore,
22 indicated by the appended claims and their combination in whole or in part rather than by the
23 foregoing description. All changes that come within the meaning and range of equivalency
24 of the claims are to be embraced within their scope.

25 What is claimed and desired to be secured by United States Letters Patent is:

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